REMARKS

In response to the Office Action mailed December 15, 2008, Applicants respectfully request reconsideration. Claims 1 and 3-30 were previously pending in this application. By this amendment, claims 1, 3-25 and 27-29 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26, and 30 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §103

I. The Office Action rejected claims 1, 3-25 under 35 U.S.C. §103(a) as being allegedly unpatentable over Lewis et al., U.S. Patent No. 5,797,043 ("Lewis") in view of George, U.S. Patent No. 6,785,829 ("George") and further in view of Lai et al., U.S. Patent No. 6,785,829 ("Lai"). Applicants respectfully disagree.

Independent Claim 1

Claim 1, as amended, recites:

> A processing system for accessing data, the processing system comprising:
> a processor comprising an execution unit for executing instructions;
> a stream register unit being part of the processor and configured to supply a first type of data from a peripheral to the execution unit of the processor, the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral;
> a FIFO coupled to the peripheral to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO coupled to the peripheral to the at least one stream register unit FIFO; and
> a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access a second type of data, the second type of data being randomly accessible data held in the data memory;
> wherein the first type of data is supplied via the communication path directly from the FIFO coupled to the peripheral to the at least one stream register unit FIFO of the stream register unit of the processor and the second type of data is supplied via the memory bus, separate from the communication path, between the data memory and the processor, and
> wherein the stream register unit is configured to:
> *in response to a request for a data item from the execution unit, when the data item in located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit*, and

when the at least one stream register unit FIFO does not contain the data item in the next location, request the data item from the FIFO coupled to the peripheral and send a stall signal to the execution unit causing the execution unit to stop executing instructions.
(Emphasis added).

On page 4, the Office Action states that the combination of Lewis and George "fails to teach a system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different system indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions." Next, the Office Action states that Lai "teaches a system, wherein the stream register unit is configured to, when the FIFO coupled to the peripheral provides, in response to a request for data from the stream register unit, an indication that the data is not available (first defer identifier, column 3, lines 16-20), send a stall signal to the execution unit, causing the execution unit to stop executing instructions (issue a stop signal, column 3, lines 20-26)."

On pages 14 and 15, in Response to Arguments provided in Applicants' previous response, the Office Action states that "the examiner notes that Lai is relied upon for the teachings of using a STOP signal when data is unavailable. Other teachings of the STOP signal were not cited by the Examiner. Clearly from the cited passages in column 3, lines 16-26 one of ordinary skill in the art can recognize that Lai sends a signal that causes a stop in execution when data is not available." While Lai indeed describes a stop signal, Applicants respectively assert that this signal of Lai is different from the stall signal causing the execution unit to stop executing instructions.

The cited portion of Lai reproduced here in its entirety states that "[t]he initiator issues a first request signal to use the PCI bus to access data in the responder; When the responder accepts the first request signal but can not immediately respond to the first request signal, the responder generates a first defer identifier corresponding to the first request signal; The responder issues a stop signal and the first defer identifier; *The initiator issues a second request* signal to use the PCI bus to access data in the responder; When the responder accepts the second request signal but can not immediately respond to the second request signal, the responder generates a second defer identifier corresponding to the second request signal; The responder issues a stop signal and the second defer identifier" (Lai, col. 3, lines 20-26) (emphasis added).

Nowhere in this portion (or in any other portion) does Lai state that the stop, or STOP, signal "**causes a stop in execution when data is not available,**" as asserted in the Office Action (emphasis added).

Contrary to the assertions made in the Office Action, the fact that the signal of Lai is called a "stop signal" does not necessary imply that Lai describes that some "execution" is stopped. Indeed, Lai only discusses that when the responder accepts the first request signal but can not immediately respond to the first request signal, the responder... issues a stop signal and the first defer identifier (Lai, col. 3, lines 16-21). Next, when the initiator issues a second request signal to use the PCI bus to access data in the responder and the responder accepts the second request signal but can not immediately respond to the second request signal, the responder ... issues a stop signal and the second defer identifier (Lai, col. 3, lines 22-28).

Further, it is not clear to what component of Lai the Office Action refers to when stating that the stop signal of Lai "causes a stop in execution." It is clear that in Lai the initiator is not "stopped" after the responder issues a stop signal, at least for the reason that, when the stop signal is issued, the initiator **issues a second** request signal (emphasis added). The responder of Lai is not stopped either. In addition, Lai clearly defines the purpose of issuing a stop signal by the responder. Thus, Lai states that in cycle T5 , the responder 32 asserts a stop signal STOP, acknowledging the initiator 30a to **deassert the FRAME signal** (emphasis added) (Lai, col. 6, lines 1-3). Lai describes that a FRAME signal is asserted by the initiator to indicate that data transfer is under way (col. 2, lines 11-13). Thus, as would be understood by one of skill in the art, **deasserting** the FRAME **signal** is different from sending a stall signal to the execution unit of the processor causing the execution unit to stop executing instructions, as recited in claim 1. In addition, in Lai, the initiators are the PCI-compatible peripheral devices connected to the PCI bus (col. 4, lines 54-56). In contrast, claim 1 recites that the stream register unit is configured to: in response to a request for a data item *from the execution unit* ... when the at least one stream register unit FIFO does not contain the data item in the next location, request the data item *from the FIFO coupled to the peripheral* (emphasis added).

Furthermore, claim 1 has been amended to recite that the stream register unit is configured to: in response to a request for a data item from the execution unit, when the data item in located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit, and when the at least one stream register unit FIFO does not contain

the data item in the next location, request the data item from the FIFO coupled to the peripheral and send a stall signal to the execution unit causing the execution unit to stop executing instructions. None of the cited references teaches or suggest these limitations.

In view of the foregoing, claim 1 patentably distinguishes over Lewis, George and Lai, either alone or in combination.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-23 is respectfully requested.

Independent Claim 24

Claim 24, as amended, recites:

> A streaming data handling system, comprising:
> a processor comprising an execution unit for executing instructions;
> a stream register being part of the processor and configured to supply data from a peripheral to the processor, the stream register including at least one stream register FIFO configured to store the data received from the peripheral; and
> a FIFO memory coupled to the peripheral to receive the data from the peripheral and connected to the least one stream register FIFO via a communication path,
> wherein the stream register and the FIFO memory operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order, and
> wherein the stream register is configured to:
> *in response to a request for a data item from the execution unit, when the data item in located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit*, and
> *when the at least one stream register unit FIFO does not contain the data item in the next location, request the data item from the FIFO coupled to the peripheral and send a stall signal to the execution unit causing the execution unit to stop executing instructions.*
> (Emphasis added).

On pages 2-5, the Office Action rejects claim 24 for the same reasons as claim 1. As should be clear from the above discussion, none of the cited references teaches all of the limitations of claim 24.

In view of the foregoing, claim 24 patentably distinguishes over Lewis, George and Lai, either alone or in combination.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 24 and 25 is respectfully requested.

II. The Office Action rejected claims 26-30 (including independent claims 26 and 30) under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis in view of Garcia et al. (U.S. Patent No. 6,433,785) ("Garcia"). Applicants respectfully disagree.

Independent Claim 26

Claim 26 recites:

> A stream register being part of a processor comprising an execution unit, the stream register being coupled between the execution unit and a peripheral and comprising:
> a receiver arranged to receive a request for a data item from the execution unit; and
> at least one FIFO configured to store the data item received from the peripheral; wherein the stream register is arranged to:
> receive the request for the data item;
> determine whether the requested data item is in the at least one FIFO;
> when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and
> send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, when the data item is available, send the data item to the processor, and, when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

Applicants note that the Office Action appears not to address claims 26 and 30 as currently pending. On pages 11-12, while rejecting claims 26 and 30, the Office Action states that "Lewis teaches a stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and peripheral and between the execution unit and a memory, comprising:

a receiver arranged to receive a request for a data item from the execution unit (column 10, lines 30-41); at least one FIFO configured to store the data item received form [sic] the peripheral (FIFO pool 172, figure 5a); and a stream engine (element 76, figure 3), arranged to

send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item (I/O Channel Controller, element 62, figure 3), and, when the data item is available (available space and data, Table VII sent via BTU, element 170 figure 5b.), send the data item to the execution unit of the processor."

Claim 26 recites, inter alia, "the stream register is arranged to: *receive the request for the data item; determine whether the requested data item is in the at least one FIFO; when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor*" (emphasis added). The Office Action does not mention these limitations of claim 26.

Further, while on page 11 the Office Action states that Lewis **teaches** a stream register being part of a processor. At the same time, on page 4, the Office Action concedes that Lewis **fails to teach** a system wherein a stream register unit being part of the processor. These statements appear to be contradictory.

The Office Action concedes that Lewis fails to teach "a register wherein when the data item being requested is not available, sending a timeout signal to the processor." The Office Action then states that Garcia teaches a register wherein when the data item being requested is not available, sending a timeout signal to the execution unit of the processor (timeout counter, column 5, lines 26-42). Claim 26 recites "when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request."

On page 15, in Response to Arguments provided in Applicants' previous response, the Office Action states that "the applicant has elaborated on alternate embodiments of Garcia to show that the timeout signal may vary from that of instant application how explicitly pointing out differences in the specification without have such characteristics necessitated by the claims does not overcome the rejection." While this statement is not entirely clear, Applicants again respectfully note that Garcia does not describe a timeout signal as recited in claims 26 and 30. Claim 26 recites sending a timeout **signal** to the execution unit of the processor **causing the processor to interrupt such that it can execute tasks other than the request** (emphasis added). Simply because both Garcia and claim 26 use the word "timeout," does not indicate that the timeout counter of Garcia and the timeout signal recited in claim 26 are identical.

Garcia is directed to a memory controller that improves processor to graphics device throughput by reducing the frequency of retries of postable write transaction requests (Abstract). In Garcia, the bus interface unit initiates the timeout counter if the bus interface unit is currently unable to complete the first postable write transaction request due to unavailability of the posted write buffer and if a second transaction request is received (col. 2, lines 21-24). The bus interface unit issues *a retry* response to the first posted write transaction request *upon an expiration of the timeout counter* if the posted write buffer remains unavailable (emphasis added) (Garcia, col. 2, lines 25-28). Thus, Garcia does not teach or suggest "when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor," as recited in claim 26.

Further, as should be understood by one of skill in the art, in Garcia, the timeout counter is initiated to reduce the number of retries of postable write transaction requests that can degrade graphics subsystem performance (*See*, for example, Garcia, col. 2, lines 1-3). In contrast, claim 26 recites sending "a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request." In addition, the postable write transaction requests are requests to **write** data into the posted write buffer, which is different from "the request for the data item" recited in claim 26 (emphasis added). Thus, Garcia states that when the processor 110 initiates a transaction to **write** data to the graphics device 140, it issues a first **postable write transaction request** (col. 3, lines 46-48) (emphasis added). The availability of the posted write buffer is also different from "when the requested data item is not in the at least one FIFO" of the stream register, as recited in claim 26.

Therefore, the timeout counter of Garcia is different from timeout signal recited in claim 26. In view of the above, contrary to the assertions made in the Office Action, Garcia does not teach or suggest sending a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request, as recited in claim 26.

In view of the foregoing, claim 26 patentably distinguishes over Lewis and Garcia, either alone or in combination.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-29 is respectfully requested.

Independent Claim 30

Claim 30 recites:

> A stream register being part of a processor comprising an execution unit, the stream register being coupled between the execution unit and a memory, the stream register comprising:
>
> a receiver arranged to receive a request for a data item from the execution unit of the processor; and
>
> at least one FIFO configured to store the data item received from a peripheral; wherein the stream register is arranged to:
>
> receive the request for the data item;
>
> determine whether the requested data item is in the at least one FIFO;
>
> when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor; and
>
> send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, when the data item is available, send the data item to the execution unit of the processor, and, when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request.

On pages 11-12, the Office Action rejects claim 30 for the same reasons as claim 26. As discussed above, the Office Action does not address claim 30 as currently pending. Further, as should be clear from the above discussion, none of the cited references teaches all of the limitations of claim 30.

In view of the foregoing, claim 30 patentably distinguishes over Lewis and Garcia, either alone or in combination.

Accordingly, withdrawal of the rejection of claim 30 is respectfully requested.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance. A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, the Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 23/2825, under Docket No. S1022.81044US00.

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Respectfully submitted,

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